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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,859	08/02/2001	Hans Jurgen Mattausch	212005US2	4187

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	6

DATE MAILED: 07/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,859	MATTAUSCH ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,13,14,16,23,25,31-40,49 and 50* is/are rejected.

7)☒ Claim(s) *2,5,7-12,15,17-22,24,26-30,41-48,51 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to Application No. 10/056,293 filed August 02, 2001. Claims 1-52 are pending in this application.

2. The specification and the claims have been examined with the results that follow.

Claim Objections

3. Claims 1-52 are objected to because of the following informalities:

In claim 1, lines 4 and 10, please delete –the-- since there was no previous mention of cache line indices in the claim.

In claim 1, lines 4 and 11, it is not clear if "each" represents the "memories" or "the blocks" or "the cache line indices".

In claim 1, line 11, please delete –the-- since there was no previous mention of "cache line offsets" in the claim.

In claim 1, line 14, please delete –the-- since there was no previous mention of "write and read conflicts" in the claim.

Claim 2, directly dependent on claim 1, is objected to for the reasons stated above.

In claim 3, lines 3 and 5, it appears that "comparing the tags" should be replaced with –comparing tags--, and "with the tags" should be replaced with –with tags--. There is no previous mention of tags being supplied in the claim or its parent claim.

In claim 4, line 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 5, line 3, before "said N-port data memories", please insert –and--.

In claim 5, line 7, it appears that "the address" should be replaced with –an address--, and "the tag" should be replaced with –a tag--.

In claim 5, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 5, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 6, line 3, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 7, lines 2 and 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 8, lines 3 and 5, it appears that "comparing the tags" should be replaced with –comparing tags--, and "with the tags" should be replaced with –with tags--. There is no previous mention of tags being supplied in the claim or its parent claims.

In claim 9, line 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 10, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 10, line 8, it appears that "the address" should be replaced with –an address--.

In claim 10, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 11, line 3, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 12, lines 2 and 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 13, line 4, before "write data and read data", please delete –the-- since there was no previous mention of "write data and read data" in the claim.

In claim 14, line 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 15, line 7, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 15, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 15, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 16, line 3, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 17, lines 2 and 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 18, line 4, before "write data and read data", please delete –the-- since there was no previous mention of "write data and read data" in the claim or its parent claims.

In claim 19, line 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 20, line 7, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 20, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 20, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 21, line 3, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 22, lines 2 and 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 23, line 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 24, line 7, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 24, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 24, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 25, line 3, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 26, line 2, it appears that "tag memory" should be replaced with –tag memories--.

In claim 27, line 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 28, line 7, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 28, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 28, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 29, line 3, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 30, lines 2 and 4, it appears that "tag memory" and "data memory" should be replaced with –tag memories-- and –data memories--.

In claim 31, line 13, before "for each of the N ports", please delete –and--.

In claim 33, line 7, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 33, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 33, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

Claims 32, 34 and 35, directly dependent on claim 31, are objected to for the reasons stated above.

In claim 36, line 12, before "for each of the N ports", please delete –and--.

In claim 38, lines 7-8, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 38, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 38, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

Claims 37, 39 and 40, directly dependent on claim 36, are objected to for the reasons stated above.

In claim 41, line 22, it appears that "circuits" should be replaced with –circuit--.

In claim 41, lines 20 and 26, after "cell blocks", please delete --,--.

In claim 41, line 22, after "transition circuit", please delete --,--.

Claims 42 and 44, directly dependent on claim 41, are objected to for the reasons stated above.

In claim 43, line 3, it appears that "or pair" should be replaced with –a pair--.

In claim 43, line 4, it appears that "to form combined" should be replaced with –to form a combined--.

In claim 43, line 7-8, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 43, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 43, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 45, line 24, it appears that "circuits" should be replaced with –circuit--.

In claim 45, line 24, after "transition circuit", please delete --,--.

In claim 45, line 28, after "cell blocks", please change "," to –and--.

In claim 45, line 29, after "core", please delete --,--.

Claims 46 and 48, directly dependent on claim 45, are objected to for the reasons stated above.

In claim 47, lines 7-8, it appears that "the address allocated to the tag" should be replaced with –an address allocated to a tag--.

In claim 47, line 9, please replace "being 0 or more" with –mtag and mword being 0 or more--.

In claim 47, line 9, it appears that "the cache line offset" should be replaced with –a cache line offset--.

In claim 49, line 15, before "for each of the N ports", please delete –and--.

In claim 50, line 15, before "for each of the N ports", please delete –and--.

In claim 51, lines 22 and 28, after "cell blocks", please delete --,--.

In claim 51, line 25, after "transition circuits", please delete --,--.

In claim 52, line 24, after "data word", please delete --,--.

In claim 52, line 26, after "transition circuits", please delete --,--.

In claim 52, line 30, after "cell blocks", please delete --,--.

In claim 52, line 26, after "core", please delete --,--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 31-35, 36-40, 49 and 50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 31, 36, 49 and 50, the phrase "for example" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claims 32-35 and 37-40 are directly or indirectly dependent on claims 31 and 36 and are rejected for the reasons stated above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1, 3-4, 6, 13, 14, 16, 23 and 25 are rejected under 35 U.S.C. 102(a) as being anticipated by applicants' Admitted Prior Art (hereinafter "APA").

As per claim 1, APA discloses a multi-port cache memory, comprising:

first to K-th N-port tag memories [*multi-port cache memory comprises 2 tag memories*; page 4, lines 6-8] each consisting of M-number of one-port cell blocks [*each of the tag storages is formed from multi-port storage cells*; page 4, lines 13-15] and of an N-port decoder for decoding the N cache line indices, each having 1 bit or more [*cache line indices are transmitted into the N-port decoder*; page 2, lines 19-23], supplied to the first to K-th tag memories [cache line indices of N*mind bits *are transmitted into the N-port decoder of the tag memory*, page 2 lines 19-21], each of K and M being an integer of 1 or more and N being an integer of more than 1 [*N ports, K=2 tag memories, M= multi-port*];

first to K-th N-port data memories [*multi-port cache memory comprises 2 data memories*; page 4, lines 6-12] each consisting of M-number of one-port cell blocks [*each of the data storages is formed from multi-port storage cells*; page 4, lines 13-15] and of an N-port decoder for decoding the N cache line indices, each having 1 bit or more [*cache line indices are transmitted into the N-port decoder*; page 2, lines 19-23], and the N cache line offsets, each having 0 bit or more, supplied to the first to K-th data memories [*the cache line offsets of*

*N*word bits are transmitted into the N-port of the data memory*; page 3, lines 9-11]; and a conflict management circuit for managing the write and read conflicts in the first to K-th N-port tag memories and the first to K-th N-port data memories [*conflict management circuit rejects the access of all but one of the conflicting ports*; page 3, lines 18-22].

As per claim 3, APA discloses the multi-port cache memory comprises first to K-th comparing circuits [*cache hit comparing circuits 30, 30a*; page 4, lines 8-9] for comparing the tags supplied to the first to K-th N-port tag memories with the tags generated from the first to K-th N-port tag memories, respectively [*comparing the tags of the accessed data to the tags stored*; page 2, lines 17-24], and a cache hit signal is transmitted for each of the N ports by supplying the outputs of the first to K-th comparing circuits to a K-input OR circuit for each of the N ports [*OR gates transmit cache hit signals*; page 4, lines 20-22].

As per claim 4, APA discloses a multi-port cache memory according to claim 1, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag memory, and said N-port data memory [*each of the tag storages 20, 20a and data storages 50, 50a is formed from multi-port storage cells*; page 4, lines 13-15].

As per claim 6, APA discloses a multi-port cache memory according to claim 1, wherein said cell blocks included in said N-port tag memory and said N-port data memory consist of L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer) [*each of the tag storages 20, 20a and data storages 50, 50a is formed from multi-port storage cells*; page 4, lines 13-15].

As per claim 13, APA discloses a multi-port cache memory according to claim 3, wherein the outputs of said first to K-th comparing circuits control first to K-th enable

circuits that permit the input and output of the write data and read data in and out of said first to K-th data memories [*enable circuits permit transmitting the data words between the data bus and the data memories upon receipt of comparison in the comparing circuits*; page 4, lines 20-27].

As per claim 14, APA discloses a multi-port cache memory according to claim 3, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag memory and said N-port data memory [*each of the tag storages 20, 20a and data storages 50, 50a is formed from multi-port storage cells*; page 4, lines 13-15].

As per claim 16, APA discloses a multi-port cache memory according to claim 1, wherein said cell blocks included in said N-port tag memory and said N-port data memory consist of L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer) [*each of the tag storages 20, 20a and data storages 50, 50a is formed from multi-port storage cells*; page 4, lines 13-15].

As per claim 23, APA discloses a multi-port cache memory according to claim 1, wherein the number M of said one-port cell blocks is less than the number N of ports of said N-port tag memory, and said N-port data memory [*each of the tag storages 20, 20a and data storages 50, 50a is formed from multi-port storage cells*; page 4, lines 13-15].

As per claim 25, APA discloses a multi-port cache memory according to claim 1, wherein said cell blocks included in said N-port tag memory and said N-port data memory consist of L-port cell blocks having the number L of ports not less than 1 and less than N ($1 \leq L < N$, L being an integer) [*each of the tag storages 20, 20a and data storages 50, 50a is formed from multi-port storage cells*; page 4, lines 13-15].

Allowable Subject Matter

8. Claims 5, 7-12, 15, 17-22, 24 and 26-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 41, 45 and 51-52 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

10. Claims 31, 36, 49-50 and their dependent claims would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach multi-port cache and managing read and write conflicts.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Pierre M. Vital
July 23, 2003